

DATA SHEET

TZA3044T; TZA3044U 1.25 Gbits/s Gigabit Ethernet postamplifiers

Objective specification
File under Integrated Circuits, IC19

1998 Jul 07

1.25 Gbits/s Gigabit Ethernet postamplifiers

TZA3044T; TZA3044U

FEATURES

- Pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range and less external component count
- Wideband operation from 1.0 kHz to 1.25 GHz typical
- Applicable in 1.25 Gbits/s Gigabit Ethernet receivers
- Single supply voltage from 3.0 to 5.5 V
- PECL (Positive Emitter Coupled Logic) compatible data outputs
- Programmable input signal level-detection to be adjusted using a single external resistor
- On-chip DC offset compensation without external capacitor
- Fully differential for excellent PSRR.

APPLICATIONS

- Digital fibre optic receiver for Gigabit Ethernet applications
- Wideband RF gain block.

GENERAL DESCRIPTION

The TZA3044 is a high gain limiting amplifier that is designed to process signals from fibre optic preamplifiers like the TZA3043. It is pin compatible with the NE/SA5224 and NE/SA5225 but with extended power supply range, and needs less external components. Capable of operating at 1.25 Gbits/s, the chip has input signal level detection with a user-programmable threshold. The data and level-detection status outputs are differential outputs for optimum noise margin and ease of use.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3044T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TZA3044U	naked die	die in waffle pack carriers; die dimensions 1.58 × 1.58 mm	–

BLOCK DIAGRAM

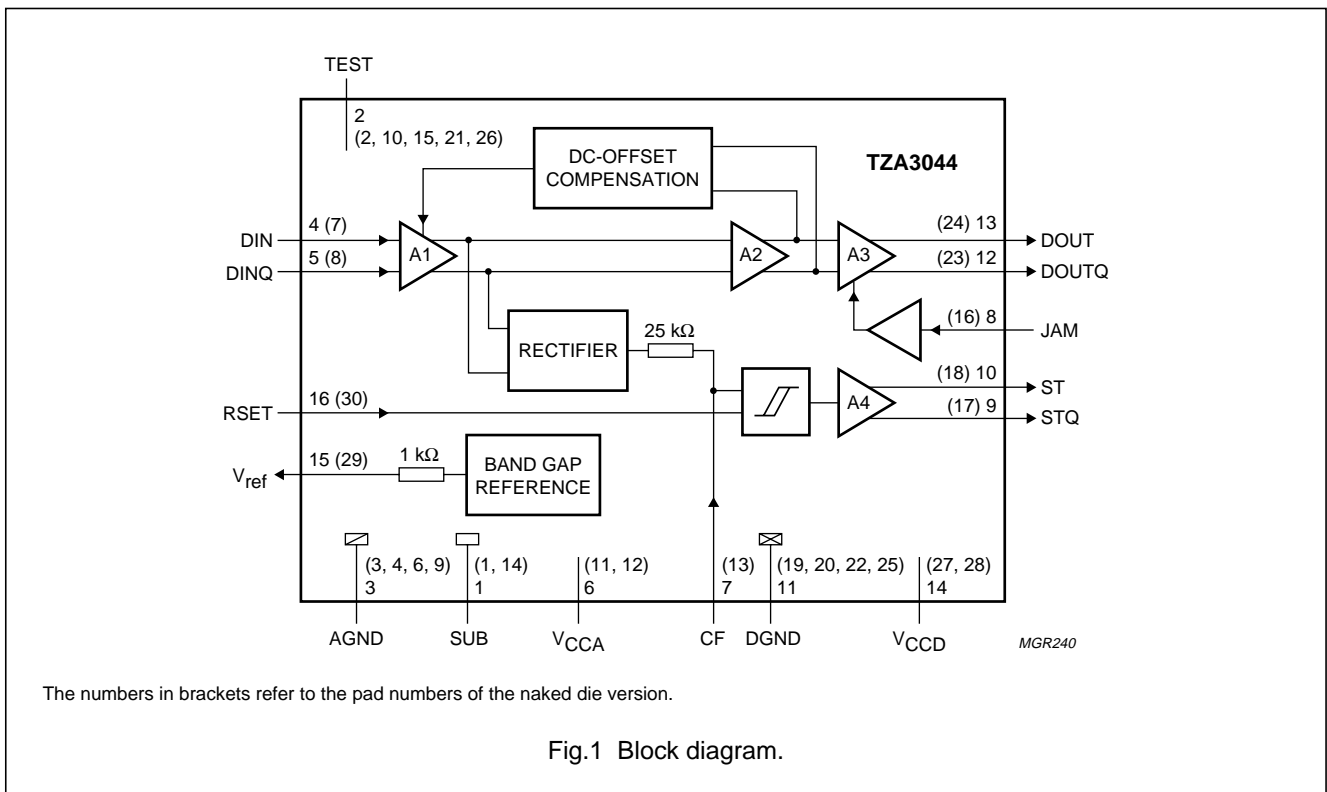


Fig.1 Block diagram.

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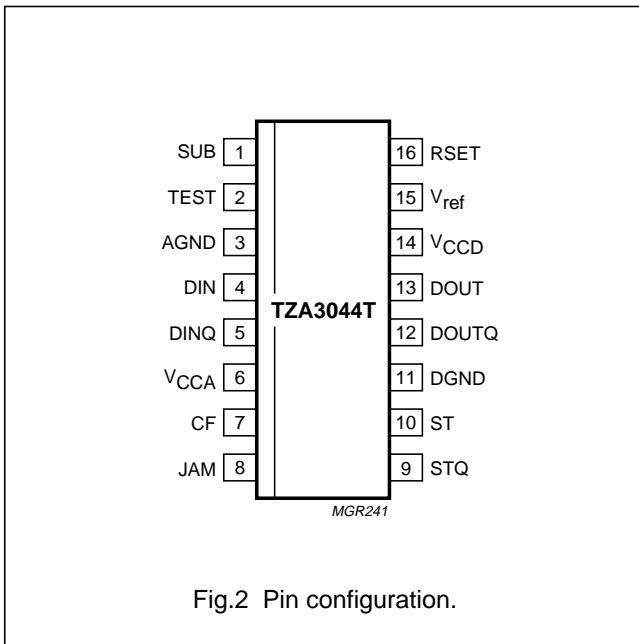
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PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
SUB	1	substrate	substrate pin; must be at the same potential as AGND (pin 3)
TEST	2	test pin	for test purpose only; to be left open in the application
AGND	3	ground	analog ground; must be at the same potential as DGND (pin 11)
DIN	4	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DINQ (pin 5)
DINQ	5	analog input	differential input; DC bias level is set internally at approximately 2.55 V; complimentary to DIN (pin 4)
V _{CCA}	6	supply	analog supply voltage; must be at the same potential as V _{CCD} (pin 14)
CF	7	analog input	filter capacitor for input signal level detector; capacitor should be connected between this pin and V _{CCA} (pin 6)
JAM	8	PECL input	PECL-compatible input; controls the output buffers DOUT and DOUTQ (pins 13 and 12). When a LOW signal is applied, the outputs will follow the input signal. When a HIGH signal is applied, the DOUT and DOUTQ pins will latch into LOW and HIGH states, respectively. When left unconnected, this pin is actively pulled LOW (JAM OFF).
STQ	9	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is HIGH; complimentary to ST (pin 10)
ST	10	PECL output	PECL-compatible status output of the input signal level detector; when the input signal is below the user-programmed threshold level, this output is LOW; complimentary to STQ (pin 9)
DGND	11	ground	digital ground; must be at the same potential as AGND (pin 3)
DOUTQ	12	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a HIGH condition; complimentary to DOUT (pin 13)
DOUT	13	PECL output	PECL-compatible differential output; when JAM is HIGH, this pin will be forced into a LOW condition; complimentary to DOUTQ (pin 12)
V _{CCD}	14	supply	digital supply voltage; must be at the same potential as V _{CCA} (pin 6)
V _{ref}	15	analog output	band gap reference voltage; typical value is 1.2 V; internal series resistor of 1 k Ω
RSET	16	analog input	input signal level detector programming; nominal DC voltage is V _{CCA} – 1.5 V; threshold level is set by connecting an external resistor between RSET and V _{CCA} or by forcing a current into RSET; default value for this resistor is 180 k Ω which corresponds with approximately 4 mV (p-p) differential input signal

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PAD CONFIGURATION

Pad centre locations

SYMBOL	PAD	COORDINATES ⁽¹⁾	
		x	y
SUB	1	-235.7	+647.8
TEST	2	-392.8	+647.8
AGND	3	-532.8	+647.8
AGND	4	-647.8	+507.1
n.c.	5	-647.8	+350.0
AGND	6	-647.8	+210.0
DIN	7	-647.8	+70.0
DINQ	8	-647.8	-70.0
AGND	9	-647.8	-210.0
TEST	10	-647.8	-350.0
V _{CCA}	11	-647.8	-507.1
V _{CCA}	12	-532.8	-647.8
CF	13	-392.8	-647.8
SUB	14	-235.7	-647.8
TEST	15	-78.6	-647.8
JAM	16	+61.4	-647.8
STQ	17	+218.5	-647.8
ST	18	+375.6	-647.8
DGND	19	+532.7	-647.8
DGND	20	+647.8	-507.1
TEST	21	+647.8	-350.0
DGND	22	+647.8	-210.0
DOUTQ	23	+647.8	-70.0
DOUT	24	647.8	70.0
DGND	25	647.8	210.0
TEST	26	647.8	350.0
V _{CCD}	27	647.8	507.1
V _{CCD}	28	532.7	647.8
V _{ref}	29	392.7	647.8
RSET	30	235.6	647.8
n.c.	31	78.5	647.8
n.c.	32	-78.6	+647.8

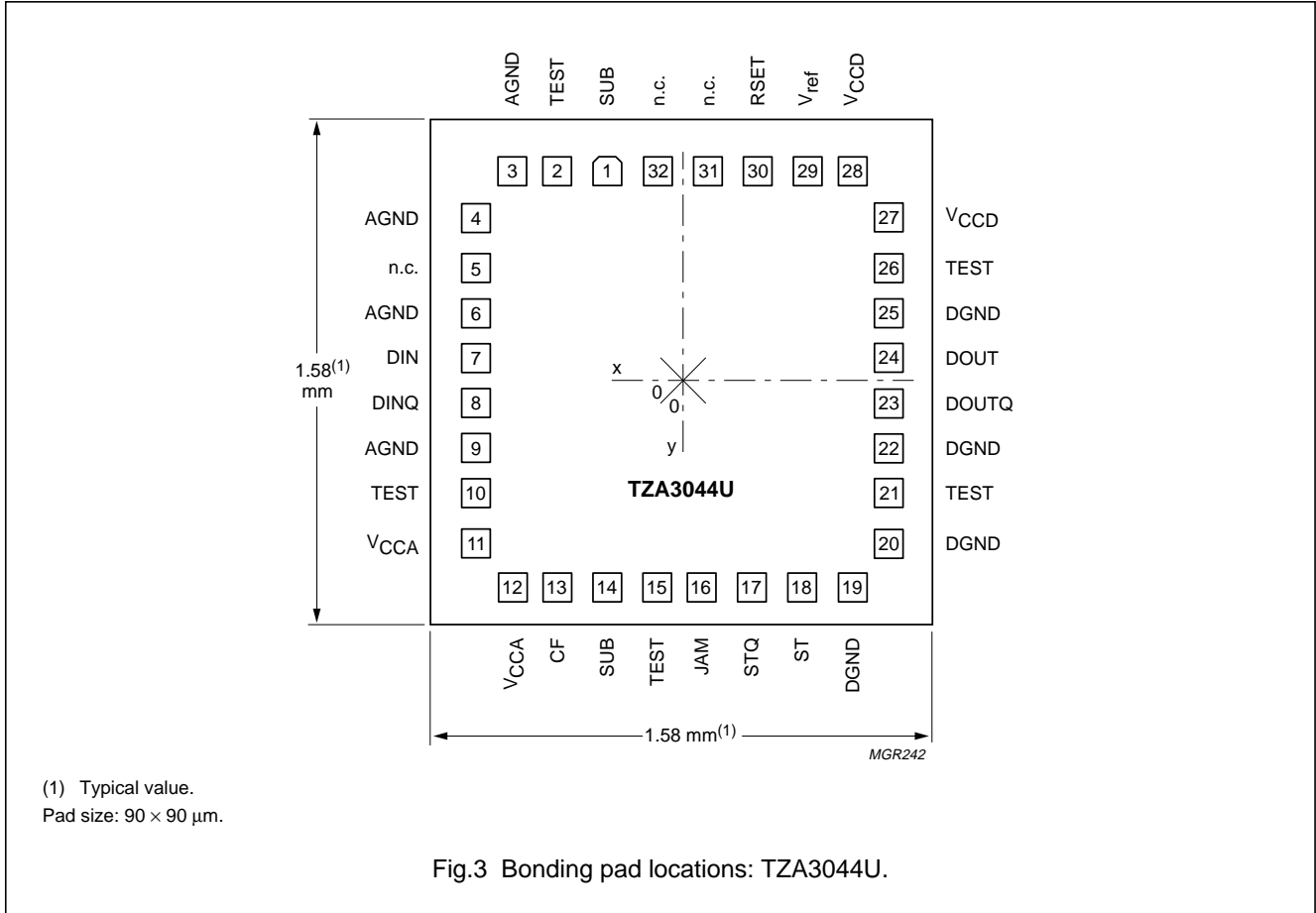
Note

- Coordinates represent the position of the centre of the pad, in μm , with respect to the centre of the die.

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Bonding pad locations



FUNCTIONAL DESCRIPTION

The TZA3044 accepts up to 1.25 Gbits/s Gigabit Ethernet data streams, with amplitudes from 2 mV (p-p) up to 1 V (p-p) single-ended. The input signal will be amplified and limited to differential PECL output levels (see Fig.1).

The input buffer A1 presents an impedance of approximately 4.5 kΩ to the data stream on the inputs DIN and DINQ. The input can be used both single-ended and differential, but differential operation is preferred for better performance.

Because of the high gain of the postamplifier, a very small offset voltage would shift the decision level in such a way that the input sensitivity decreases drastically. Therefore a DC offset compensation circuit is implemented in the TZA3044, which keeps the input of buffer A3 at its toggle point in the absence of any input signal.

An input signal level detection is implemented to check if the input signal is above the user-programmed level.

The outcome of this test is available at the PECL outputs ST and STQ. This flag can also be used to prevent the PECL outputs DOUT and DOUTQ from reacting to noise in the absence of a valid input signal, by connecting the output STQ to the input JAM. This insures that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit error rate system operation.

PECL logic

The logic level symbol definitions for PECL are shown in Fig.4.

Input biasing

The input pins DIN and DINQ are DC biased at approximately 2.55 V by an internal reference generator (see Fig.5). The TZA3044 can be DC coupled, but AC coupling is preferred. In case of DC coupling, the driving source must operate within the allowable input signal range (2.0 V to V_CCA + 0.5 V). Also a DC offset voltage of

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more than a few millivolt should be avoided, since the internal DC offset compensation circuit has a limited correction range.

If AC coupling is used to remove any DC compatibility requirement, the coupling capacitors must be large enough to pass the lowest input frequency of interest. For example, 1 nF coupling capacitors react with the internal 4.5 kΩ input bias resistors to yield a lower -3 dB frequency of 35 kHz. This then sets a limit on the maximum number of consecutive pulses that can be sensed accurately at the system data rate. Capacitor tolerance and resistor variation must be included for an accurate calculation.

DC-offset compensation

A control loop connected between the inputs of buffer A3 and amplifier A1 (see Fig.1) will keep the input of buffer A3 at its toggle point in the absence of any input signal. Because of the active offset compensation which is integrated in the TZA3044, no external capacitor is required. The loop time constant determines the lower cut-off frequency of the amplifier chain, which is set at approximately 850 Hz.

Input signal level-detection

The TZA3044 allows for user-programmable input signal level-detection and can automatically disable the switching of the PECL outputs if the input signal is below a set threshold. This prevents the outputs from reacting to noise in the absence of a valid input signal, and insures that data will only be transmitted when the signal-to-noise ratio of the input signal is sufficient for low bit-error-rate system operation. Complementary PECL flags (ST and STQ) indicate whether the input signal is above or below the programmed threshold level.

The input signal is amplified and rectified before being compared to a programmable threshold reference. A filter is included to prevent noise spikes from triggering the level-detector. This filter has a nominal 1 μs time constant and additional filtering can be achieved by using an external capacitor between pin CF and V_{CCA} (the internal driving impedance nominally is 25 kΩ). The resultant signal is then compared to a threshold current through pin RSET (see Fig.6). This current can be set by connecting an external resistor R_{DETECT} between pin RSET and V_{CCA}, or by forcing a current into pin RSET.

The relationship between the threshold current and the detected input voltage is approximately:

$$I_{RSET} = 0.002 \times (V_{DIN} - V_{DINQ}) \text{ [A]} \quad (1)$$

Since the voltage on pin RSET is held constant at 1.5 V below V_{CCA}, the current flowing into this pin will be:

$$I_{RSET} = \frac{1.5}{R_{DETECT}} \text{ [A]} \quad (2)$$

Combining these two formulas results in a general formula to calculate R_{DETECT} for a given input signal level-detection:

$$R_{DETECT} = \frac{750}{(V_{DIN} - V_{DINQ})} \text{ [}\Omega\text{]} \quad (3)$$

In this formula, V_{DIN} and V_{DINQ} are in V (p-p).

Example: Detection should occur if the differential voltage of the input signals drops below 4 mV (p-p). In this case, a reference current of 0.002 × 0.004 = 8 μA should flow into pin RSET. This can be set using a current source or simply by connecting a resistor of the appropriate value. The resistor must be connected between V_{CCA} and pin RSET. In this example the resistor would be:

$$R_{DETECT} = \frac{750}{0.004} = 187.5 \text{ k}\Omega$$

The hysteresis is fixed internally at 3 dB electrical. In the example of above, a differential level below 4 mV (p-p) of the input signal will drive pin ST to LOW, and an input signal level above 5.7 mV (p-p) will drive pin ST to HIGH.

Since a JAM function is provided which forces the data outputs to a predetermined state (DOUT = LOW and DOUTQ = HIGH), the pins STQ and JAM can be connected to automatically disable the signal transmission when the chip senses that the input signal is below the programmed threshold.

Response time of the input signal level-detection circuit is determined by the time constant of the input capacitors, together with the filter time constant (1 μs internal plus the additional capacitor at pin CF).

PECL output circuits

The output circuit of ST and STQ is given in Fig.7

The output circuit of DOUT and DOUTQ is given in Fig.8.

Some PECL termination schemes are given in Fig.9.

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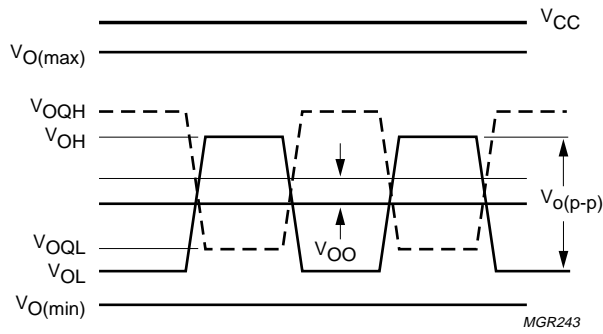


Fig.4 Logic level symbol definitions for PECL.

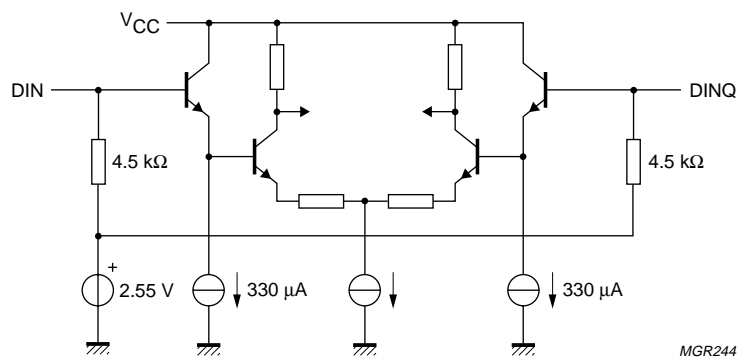


Fig.5 Data input circuit DIN and DINQ.

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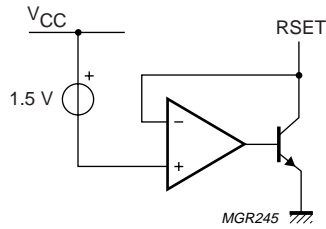


Fig.6 Level-detect input circuit RSET.

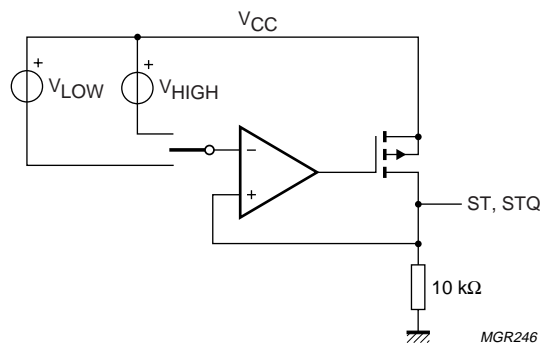


Fig.7 PECL output circuit ST and STQ.

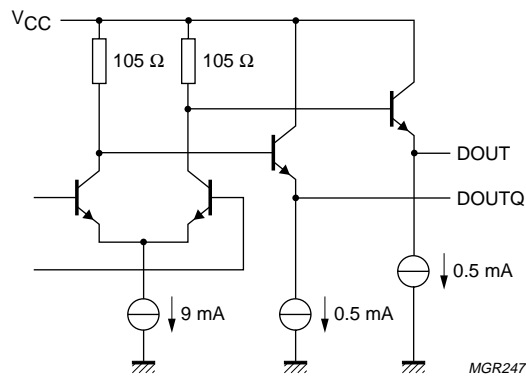


Fig.8 PECL output circuit DOUT and DOUTQ.

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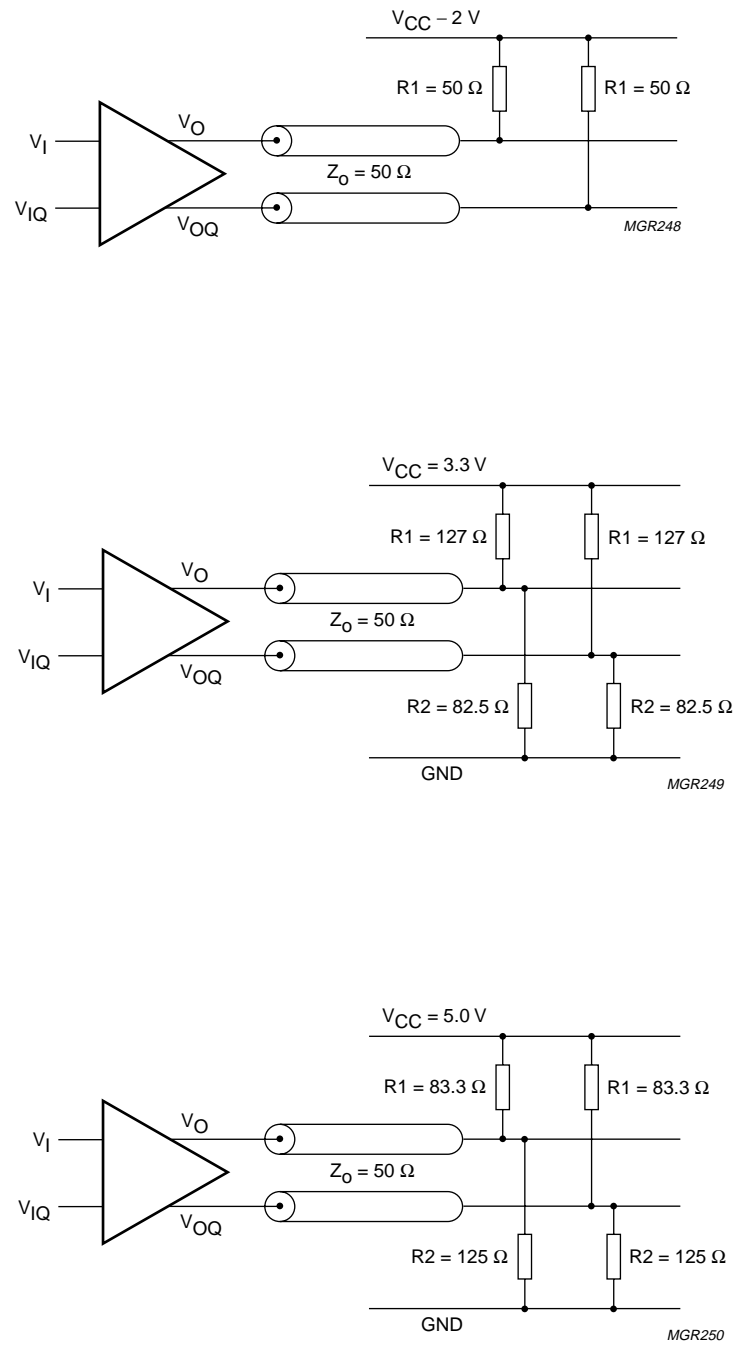


Fig.9 PECL output termination schemes.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{CC}	supply voltage		-0.5	+6	V
V _n	DC voltage pins 4 and 5 (7 and 8): DIN and DINQ pin 7 (13): CF pin 8 (16): JAM pins 9, 10, 12 and 13 (17, 18, 23 and 24): STQ, ST, DOUTQ and DOUT pin 15 (29): V _{ref} pin 16 (30): RSET	note 1	-0.5 -0.5 -0.5 V _{CC} - 2 -0.5 -0.5	V _{CC} + 0.5 V _{CC} + 0.5 V _{CC} + 0.5 V _{CC} + 0.5 +3.2 V _{CC} + 0.5	V V V V V V
I _n	DC current pin 4 and 5 (7 and 8): DIN and DINQ pin 7 (13): CF pin 8 (16): JAM pins 9, 10, 12 and 13 (17, 18, 23 and 24): STQ, ST, DOUTQ and DOUT pin 15 (29): V _{ref} pin 16 (30): RSET	note 1	-1 -1 -1 -25 -2 -2	+1 +1 +1 +10 +2.5 +2	mA mA mA mA mA mA
P _{tot}	total power dissipation		-	tbf	mW
T _{stg}	storage temperature		-65	+150	°C
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-40	+85	°C

Note

1. The numbers in brackets refer to the pad numbers of the naked die version.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th(j-s)}	thermal resistance from junction to solder point	tbf	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	tbf	K/W

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CHARACTERISTICS

For typical values $T_{amb} = 25\text{ °C}$ and $V_{CC} = 3.3\text{ V}$; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CC}	supply voltage		3	3.3	5.5	V
I_{CCD}	digital supply current	note 1	–	18	27	mA
I_{CCA}	analog supply current		–	15	22	mA
P_{tot}	total power dissipation	note 1	–	110	270	mW
T_j	junction temperature		–40	–	+120	°C
T_{amb}	ambient temperature		–40	+25	+85	°C
Inputs: DIN and DINQ						
$V_{i(se)(p-p)}$	input signal voltage single-ended (peak-to-peak)		0.002	–	1.0	V
$V_{i(dif)(p-p)}$	input signal voltage differential (peak-to-peak)		0.004	–	2.0	V
V_I	absolute input signal voltage		2.1	2.55	$V_{CCA} + 0.5$	V
$V_{IO(eq)}$	equivalent input signal offset voltage		–	–	50	μV
$V_{IO(cor)}$	input offset voltage correction range	note 2	–5	–	+5	mV
R_i	input resistance	single-ended	2.9	4.5	7.6	$\text{k}\Omega$
C_i	input capacitance	single-ended	–	–	2.5	pF
$V_{n(i)(rms)}$	equivalent input RMS noise voltage	note 3	–	115	145	μV
Input signal level-detect: RSET						
I_{ref}	reference current	note 4	5	–	60	μA
V_{ref}	reference voltage	referred to V_{CCA}	–1.55	–1.5	–1.45	V
$V_{th(p-p)}$	programmability (single-ended, peak-to-peak)	$V_I = 200\text{ kHz}$ square wave	2	–	12	mV
hys	hysteresis	electrically measured	2	3	4	dB
R_F	filter resistance		14	25	41	$\text{k}\Omega$
t_F	filter time constant	$CF = 0$	0.5	1.0	2.0	μs
PECL outputs: DOUT and DOUTQ						
V_{OL}	LOW-level output voltage	$R_L = 50\ \Omega$ to $V_{CC} - 2\text{ V}$	$V_{CC} - 1840$	–	$V_{CC} - 1620$	mV
V_{OH}	HIGH-level output voltage	$R_L = 50\ \Omega$ to $V_{CC} - 2\text{ V}$	$V_{CC} - 1100$	–	$V_{CC} - 900$	mV
t_r	rise time	20% to 80%	–	150	250	ps
t_f	fall time	80% to 20%	–	100	200	ps
$t_{w(p-p)}$	pulse width distortion		–	–	30	ps
$f_{-3dB(l)}$	low frequency –3 dB point		–	0.85	1.5	kHz
$f_{-3dB(h)}$	high frequency –3 dB point		1000	1300	1600	MHz

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PECL outputs: ST and STQ						
V _{OL}	LOW-level output voltage	R _L = 50 Ω to V _{CC} - 2 V	V _{CC} - 1840	-	V _{CC} - 1620	mV
V _{OH}	HIGH-level output voltage	R _L = 50 Ω to V _{CC} - 2 V	V _{CC} - 1100	-	V _{CC} - 900	mV
t _r	rise time	20% to 80%	-	-	600	ns
t _f	fall time	80% to 20%	-	-	200	ns
PECL input: JAM						
V _{IL}	LOW-level input voltage		-	-	V _{CC} - 1490	mV
V _{IH}	HIGH-level input voltage		V _{CC} - 1165	-	-	mV
I _{I(JAM)}	JAM input current	note 5	-10	-	+10	μA
Reference voltage output: V_{ref}						
V _{ref}	reference voltage	note 6	1.165	1.20	1.235	V

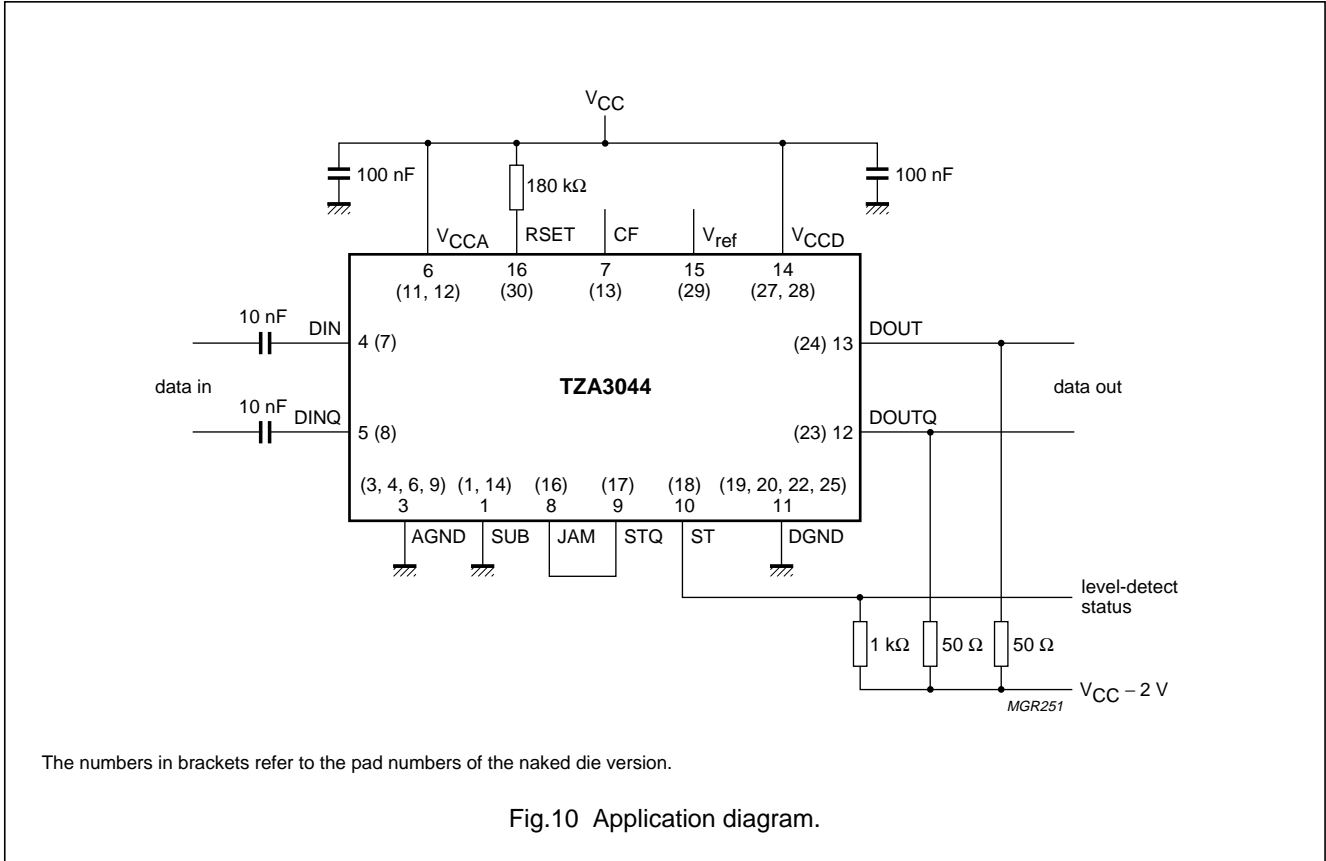
Notes

1. DOUT, DOUTQ, ST and STQ outputs are left unconnected.
2. If the input is DC coupled, the preceding amplifier's output offset voltage should not exceed these limits, in order to avoid malfunctioning of the DC offset compensation circuit.
3. Input RMS noise = $\frac{\text{total output RMS noise}}{\text{low frequency gain}}$
4. The reference currents can be set by a resistor between V_{CCA} and pin RSET. The corresponding input signal level-detect range is from 2 to 12 mV (p-p) single-ended. See section "Input signal level-detection" for detailed information.
5. Internal pull-down resistor of 500 kΩ to DGND.
6. Internal series resistor of 1 kΩ.

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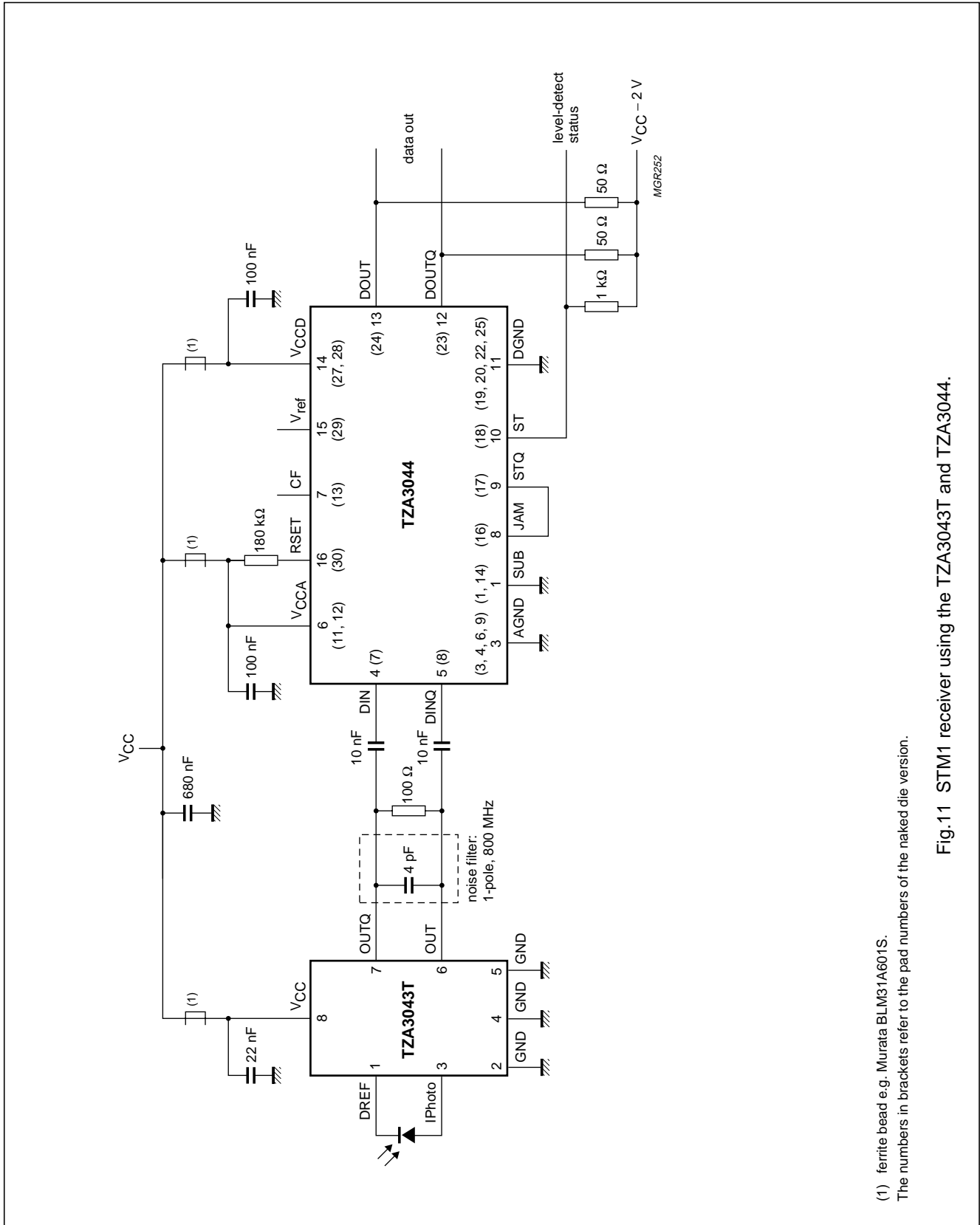
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APPLICATION INFORMATION



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(1) ferrite bead e.g. Murata BLM31A601S.
The numbers in brackets refer to the pad numbers of the naked die version.

Fig.11 STM1 receiver using the TZA3043T and TZA3044.

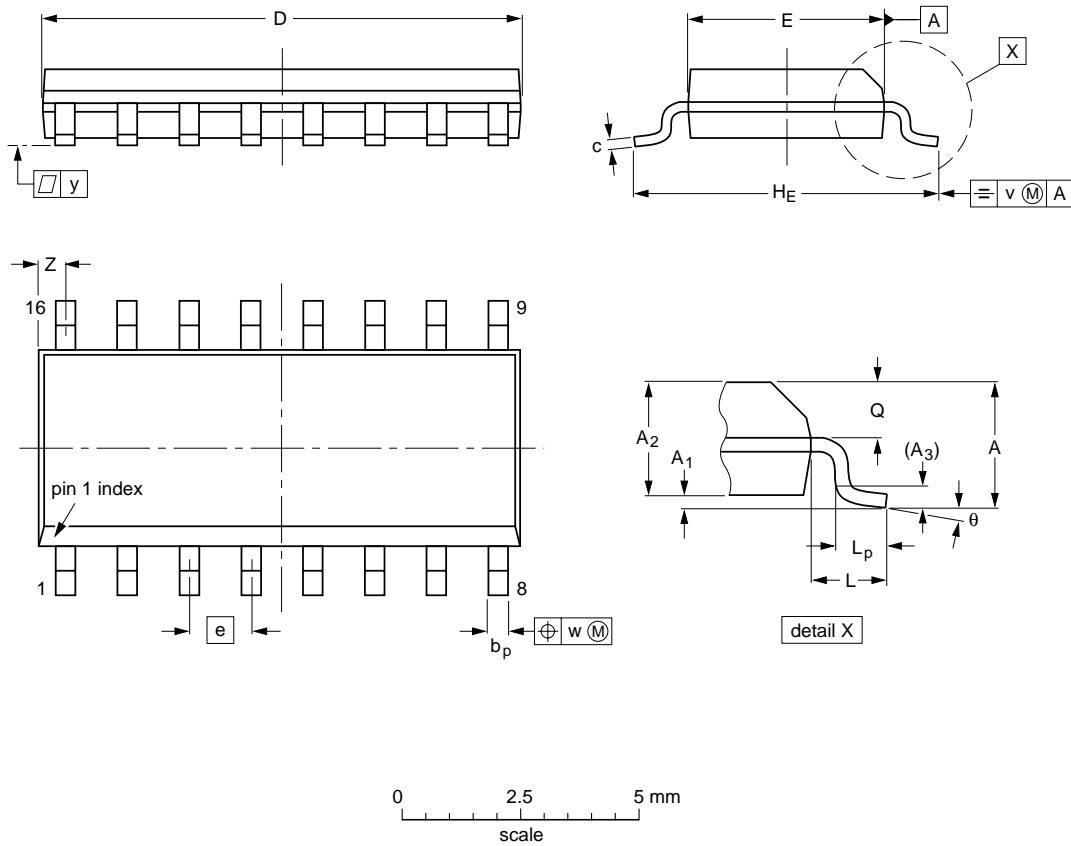
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PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT109-1	076E07S	MS-012AC			95-01-23 97-05-22

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

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